WE CLAIM:

1. A method for testing a semiconductor wafer, the semiconductor wafer having a plurality of die, comprising the steps of:

(a) coupling an array of probes to the semiconductor wafer; and thereafter

(b) applying a voltage difference across a plurality of adjacent bitline pairs and/or wordline pairs of one or more static random access memory (SRAM) arrays of at least one die of the semiconductor wafer, the voltage being larger than an operational supply voltage for the one or more SRAM arrays, to thereby induce failure of metal stringers or defects.

2. The method of claim 1, further comprising the step of simultaneously applying the voltage across respective pairs of substantially all parallel bitline pairs and/or wordlines pairs of the one or more SRAM arrays.

3. The method of claim 1, further comprising the step of simultaneously applying a voltage across respective pairs of substantially all parallel bitline pairs and/or wordlines pairs of the one or more SRAM arrays of more that one die of the semiconductor wafer.

4. The method of claim 1, further comprising the step of applying the voltage across other adjacent, parallel metal lines of the one or more SRAM arrays.

5. The method of claim 1, further comprising the step of applying the voltage at a magnitude of equal to or greater than two times the operational supply voltage.

6. The method of claim 2, further comprising the step of applying the voltage at a magnitude of equal to or greater than two times the operational supply voltage.

7. The method of claim 3, further comprising the step of applying the voltage at a magnitude of equal to or greater than two times the operational supply voltage.

8. The method of claim 4, further comprising the step of applying the voltage at a magnitude of equal to or greater than two times the operational supply voltage.

9. The method of claim 1, further comprising the step of preforming step b at an elevated temperature.

10. The method of claim 9, further comprising the step of applying the voltage at a magnitude of equal to or greater than two times the operational supply voltage.

11. The method of claim 3, further comprising the step of preforming step b at an elevated temperature.

12. The method of claim 4, further comprising the step of preforming step b at an elevated temperature.

13. A semiconductor wafer having one or more die with a static random access memory (SRAM) array integrated therein, comprising:

a test circuit integrated with the SRAM array; and

connections that couple said test circuit to the SRAM array;

wherein during probing, said test circuit applies a voltage difference across a plurality of adjacent bitline pairs and/or wordline pairs of the SRAM array, the voltage being larger than an operational supply voltage for the SRAM array, to thereby induce failure of metal stringers or defects.